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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/756,686	01/09/2001	Kazuo Matsuzaki	FUJI:179	4650

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EXAMINER
LOKE, STEVEN HO YIN

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2811	15

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/756,686	Applicant(s) MATSUZAKI ET AL.	
	Examiner Steven Loke	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *15-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *10 December 2002* is: a)☐ approved b)☒ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. The proposed drawing correction filed on 12/10/02 has been disapproved because it is not in the form of a pen-and-ink sketch showing changes in red ink or with the changes otherwise highlighted. See MPEP § 608.02(v).

2. It is unclear whether the proposed drawing correction filed on 12/10/02 is the correction of the original drawing filed on 1/9/01 or the formal drawing filed on 6/8/01. In the formal drawing filed on 6/8/01, the applicants have deleted all the reference descriptions from the figures. Appropriate correction is required.

3. Claims 2 and 9 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Fig. 13 discloses the depths of the sub-regions [159a-159c] of the offset region [159] are different from each other. The specification never discloses the depths of the sub-regions of the second region are different from each other as claimed in claim 2.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kitamura et al. (U. S. patent no. 5,705,842).

In regards to claim 1, Kitamura et al. show all the elements of the claimed invention in fig. 7. It is a semiconductor device exhibiting a high breakdown voltage,

comprising: a first region [2] of a first conductivity type (n-type); a second region [31] (region [31] on the left side of the gate electrode [7]) of a second conductivity type (p-type) formed selectively in the surface portion of the first region; a third region [8] of the first conductivity type formed selectively in the surface portion of the first region, the second region [31] and the third region [8] being spaced apart from each other; a fourth region [5] of the first conductivity type formed selectively in the surface portion of the second region; an offset region [3, 31 (regions [3, 31] formed on the right side of the gate electrode [7]), 4] of the second conductivity type formed selectively in the surface portion of the first region [2] between the second region [31] and the third region [8]; a first insulation film [6] on the offset region; a gate electrode [7] above the extended portion of the second region [31] extending between the fourth region [5] and the first region [2] with a gate insulation film [6] interposed between the extended portion of the second region [31] and the gate electrode [7]; a first main electrode [11] on the fourth region [5]; and a second main electrode [12] on the third region [8]; wherein the offset region [3, 31, 4] comprises a plurality of sub-regions [3, 31, 4] aligned between the second region [31] and the third region [8], the impurity concentrations of the sub-regions [3, 31, 4] being different from each other.

In regards to claim 4, Kitamura et al. show all the elements of the claimed invention in fig. 7. It is a semiconductor device exhibiting a high breakdown voltage, comprising: a semiconductor substrate (p-) of a second conductivity type (p- type); a first region [2] of a first conductivity type (n-type) formed selectively in the surface portion of the semiconductor substrate; a second region [31] (region [31] on the left side of the gate

electrode [7]) of a second conductivity type (p-type) formed selectively in the surface portion of the semiconductor substrate; a third region [8] of the first conductivity type formed selectively in the surface portion of the first region, the second region [31] and the third region [8] being spaced apart from each other; a fourth region [5] of the first conductivity type formed selectively in the surface portion of the second region; an offset region [3, 31 (regions [3, 31] formed on the right side of the gate electrode [7]), 4] of the second conductivity type formed selectively in the surface portion of the first region [2] between the second region [31] and the third region [8]; a first insulation film [6] on the offset region; a gate electrode [7] above the extended portion of the second region [31] extending between the fourth region [5] and the first region [2] with a gate insulation film [6] interposed between the extended portion of the second region [31] and the gate electrode [7]; a first main electrode [11] on the fourth region [5]; and a second main electrode [12] on the third region [8]; wherein the offset region [3, 31, 4] comprises a plurality of sub-regions [3, 31, 4] aligned between the second region [31] and the third region [8], the impurity concentrations of the sub-regions [3, 31, 4] being different from each other.

In regards to claims 2, 5, Kitamura et al. further disclose the depths of the sub-regions of the offset regions [3, 31, 4] are different from each other.

In regards to claims 3, 6, Kitamura et al. further disclose the gate electrode [7] is extended onto the first insulation film [6].

In regards to claims 7, 8, Kitamura et al. further disclose the impurity concentration of the sub-region [31] (region [31] on the right side of the gate electrode [7]) on the side of

the second region [31] (region [31] on the left side of the gate electrode [7]) is higher than the impurity concentration of the sub-region [4] on the side of the third region [8].

In regards to claims 9, 10, Kitamura et al. further disclose the diffusion depth of the sub-region [31] (region [31] on the right side of the gate electrode [7]) on the side of the second region [31] (region [31] on the left side of the gate electrode [7]) is deeper than the diffusion depth of the sub-region [4] on the side of the third region [8].

In regards to claims 11, 12, Kitamura et al. further disclose the impurity concentration of the sub-region [3, 31, 4] is the concentration of an impurity of the second conductivity type (p-type).

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamura et al.

In regards to claims 13 and 14, Kitamura et al. differ from the claimed invention by not showing the surface impurity concentration of the offset region of the second conductivity type is changed by adding an impurity of the first conductivity type, the amount thereof being less than the amount of the impurity of the second conductivity type in the offset region.

It would have been obvious for the surface impurity concentration of the offset region of the second conductivity type is changed by adding an impurity of the first

conductivity type and the amount thereof being less than the amount of the impurity of the second conductivity type in the offset region because it is a well known method to reduce the impurity concentration of the second conductivity type.

The process limitation of how the offset region is formed has no patentable weight in claim drawn to structure. It is important to note that there are many ways to make the offset region of the second conductivity type. Therefore, the phrase "the surface impurity concentration of the offset region of the second conductivity type is changed by adding an impurity of the first conductivity type, the amount thereof being less than the amount of the impurity of the second conductivity type in the offset region" is thus non-limiting.

8. Applicant's arguments filed 12/10/02 have been fully considered but they are not persuasive.

It is urged, in page 8 of the remarks, that Kitamura et al. never disclose an offset or fifth region that is defined by a plurality of sub-regions having different impurity concentrations. However, the sub-regions [3, 31 (regions [3, 31] formed on the right side of the gate electrode [7]), 4] are offset from the second region [31] (region [31] on the left side of the gate electrode [7]). Therefore, the sub-regions [3, 31 (regions [3, 31] formed on the right side of the gate electrode [7]), 4] are considered as the offset region of the claimed invention.

It is also urged, in page 8 of the remarks, that Kitamura's regions 3 and 31 are not offset regions because they do not become a depletion layer when the device is off. Since the claimed invention never discloses the offset region would become a depletion

layer when the device is off, it is not necessary for Kitamura et al. to show the offset region would become a depletion layer when the device is off. In addition, it is well known in the semiconductor art that the regions adjacent to a pn junction would be depleted at any bias condition. The depletion layer in regions [3, 31] would even bigger when the device is off. Therefore, Kitamura et al. inherently disclose regions [3, 31, 4] would be depleted when the device is off.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl
February 19, 2003

Steven Loke
Primary Examiner